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Keynote: Hardware/Software Co-design for AI Systems

Prof. Yiran Chen

Duke University

3:15 – 4:15 PM (CET) | August 23, 2021

The rapid growth of modern neural network (NN) models' scale generates ever-increasing demands for high computing power of artificial intelligence (AI) systems. Many specialized computing devices have been also deployed in the AI systems, forming a truly application-driven heterogenous computing platform. This talk discusses the importance of hardware/software co-design in AI system designs. We first use resistive memory based NN accelerators to illustrate the design philosophy of heterogeneous AI computing systems, and then present several hardware friendly NN model compression techniques. We also extend our discussions to distributed systems and briefly introduce the automation of co-design flow, e.g., neural architecture search. A research roadmap of our group in the relevant topics is given at the end of the talk.

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Bio

Yiran Chen received B.S (1998) and M.S. (2001) from Tsinghua University and Ph.D. (2005) from Purdue University. After five years in industry, he joined University of Pittsburgh in 2010 as Assistant Professor and then promoted to Associate Professor with tenure in 2014, held Bicentennial Alumni Faculty Fellow. He is now the Professor of the Department of Electrical and Computer Engineering at Duke University and serving as the director of NSF Industry–University Cooperative Research Center (IUCRC) for Alternative Sustainable and Intelligent Computing (ASIC) and the co-director of Duke Center for Computational Evolutionary Intelligence (CEI), focusing on the research of new memory and storage systems, machine learning and neuromorphic computing, and mobile computing systems. Dr. Chen has published one book and more than 400 technical publications and has been granted 96 US patents. He serves or served the associate editor of more than ten international academic transactions/journals and served on the technical and organization committees of numerous international conferences. He is now serving as the Editor-in-Chief of the IEEE Circuits and Systems Magazine. He received more than 20 best paper awards and nominations from international conferences and workshops. He is the recipient of the NSF CAREER award, the ACM SIGDA outstanding new faculty award, and the IEEE SYSC/CEDA TCCPS Mid-Career Award. He is a distinguished lecturer of IEEE CEDA and listed in the HPCA Hall of Fame. He is a Fellow of the ACM and IEEE.

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Keynote: Approximate Edge AI Wearables: The Path Towards Sustainability in Healthcare

Prof. David Atienza Alonso

Embedded Systems Lab. (ESL), EPFL, Switzerland

3:15 – 4:15 PM (CET) | August 24, 2021

Wearable devices are poised as the next frontier of innovation in the context of Internet-of-Things (IoT) to be able to provide personalized healthcare by interacting also with our everyday objects, which can be interconnected in ways that improve our lives and transform the medical industry. This new family of smart wearable devices provide a great opportunity for the integration of the next-generation of artificial intelligence (AI) based technologies in medical devices. However, major key challenges remain in achieving this potential due to inherent resource-constrained nature of wearable systems, coupled with their (in principle) limited computing power and data gathering requirements for Big Data medical applications, which can result in degraded and unreliable behavior and short lifetime. In this talk, Prof. Atienza will first discuss the challenges of ultra-low power (ULP) design and communication in smart wearable devices for medical applications in the context of Big Data healthcare. Then, the opportunities for edge computing and edge AI in next-generation smart wearables will be highlighted as a scalable way to fully deliver the concept of personalized medicine. This new trend of smarter wearable architectures will need to combine new ULP multi-core embedded systems with neural network accelerators, as well as including energy-scalable software layers to monitor medical pathologies by event-driven monitoring. Overall, the next-generation of smart wearable devices in the healthcare context will be able to gracefully adapt the energy consumption and precision of the pathology detection outputs according to the requirements of our surrounding world and available energy at each moment in time, as living organisms do to operate efficiently in the real world.

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Bio

David Atienza is Associate Professor of Electrical and Computer Engineering and leads the Embedded Systems Laboratory (ESL) at EPFL, Switzerland. He received his MSc and PhD degrees in Computer Science and Engineering from UCM (Spain) and IMEC (Belgium). His research interests focus on system-level design methodologies for energy-efficient computing systems, particularly multi-processor system-on-chip architectures (MPSoC) for servers and next-generation smart embedded systems for the Internet of Things (IoT) era. In these fields, he is co-author of more than 350 publications, 12 patents, and has received several best paper awards in top conferences. He was the Technical Program Chair of DATE 2015 and General Chair of DATE 2017. Dr. Atienza received among other recognitions, the ICCAD 2020 10-Year Retrospective Most Influential Paper Award, the DAC Under-40 Innovators Award in 2018, the IEEE TCCPS Mid-Career Award in 2018, an ERC Consolidator Grant in 2016, the IEEE CEDA Early Career Award in 2013, the ACM SIGDA Outstanding New Faculty Award in 2012, and a Faculty Award from Sun Labs at Oracle in 2011. He is an IEEE Fellow, an ACM Distinguished Member, and was the President (period 2018-2019) of IEEE CEDA.

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Keynote: Exploiting AI in Embedded Devices

Prof. Marian Verhelst

KU Leuven University

2:00 – 3:00 PM (CET) | August 23, 2021

Sensors are embedded more and more ubiquitously into our environment. It is however impossible to swallow all this sensory data in the cloud. This requires local processing of the sensor feed in the so-called extreme edge nodes. This is a challenge for the local nodes, which only have limited processing, memory and energy resources. This talk will give an overview of different strategies across the system stack to enable and exploit AI processing in sensory devices, ranging from low precision compute, over efficient analog processing, to runtime tuned workloads. As the resulting design and mapping space is vast, we end by present ZigZag, a design space exploration tool tuned to neural network processors.

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Bio

Marian Verhelst is an associate professor at the MICAS laboratories of the EE Department of KU Leuven and scientific director at imec. Her research focuses on embedded machine learning, hardware accelerators, HW-algorithm co-design and low-power edge processing. Before that, she received a PhD from KU Leuven in 2008, was a visiting scholar at the BWRC of UC Berkeley in the summer of 2005, and worked as a research scientist at Intel Labs, Hillsboro OR from 2008 till 2011. Marian is a member of the DATE and ISSCC executive committees, is TPC co-chair of AICAS2020 and tinyML2020, and TPC member DATE and ESSCIRC. Marian is an SSCS Distinguished Lecturer, was a member of the Young Academy of Belgium, an associate editor for TVLSI, TCAS-II and JSSC and a member of the STEM advisory committee to the Flemish Government. Marian currently holds a prestigious ERC Starting Grant from the European Union and was the laureate of the Royal Academy of Belgium in 2016.

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Keynote: Massive Federated Intelligent Reality

Wo Chang

National Institute of Standards and Technology (NIST)

7:30 – 8:30 PM (CET) | August 23, 2021

The success of AI machine learning has led to substantial improvements comparable to human performance and beyond across a variety of application domains. With the advancement of low energy small footprint Systems-on-Chip (SoC), Network-on-Chip (NoC), ML-on-Chip (MLoC) and highspeed low latency wireless communication, embedding machine learning trained models into these smart connected devices can provide localized real-time analytics given constrained environments. A vast interconnected of these devices can offer massive federated intelligence to formulate global collective insight. By leveraging these technologies with Intelligent Reality, they can transform and enhance synchronized decision-making with analytics capability to support complex environment such as smart cities, manufacturing, agriculture, video surveillance, first responder, and others. This presentation aims to foster the massive federated intelligent reality vision by understanding the current technologies landscape, future innovations, and standards development to effectively manage vast and multifaceted setting via heterogeneous smart devices within the immersive space.

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Bio

Mr. Chang is Digital Data Advisor for the NIST Information Technology Laboratory (ITL). His responsibilities include, but are not limited to, promoting a vital and growing Big Data community at NIST with external stakeholders in commercial, academic, and government sectors. Mr. Chang currently chairs the ISO/IEC JTC 1/SC 42(Artificial Intelligence)/WG 2 Working Group on Data, IEEE Big Data Governance and Metadata Management Working Group, NIST Big Data Public Working Group, General Chair for IEEE International Conference on Intelligent Reality, and NIST representative to the ISO/IEC AI standards development. Prior to joining ITL Office, Mr. Chang was manager of the Digital Media Group in ITL and his duties included overseeing several key projects in the areas of digital data, long-term preservation and management of EHRs, motion image quality, and multimedia standards. In the past, Mr. Chang was the Deputy Chair for the US National Body for MPEG (INCITS L3.1) and chaired several other key projects for MPEG and JPEG. Mr. Chang was one of the original members of the W3C's SMIL WG and developed one of the SMIL reference software.

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Keynote: IPv6-based New Internet empowering Super IoT and Next Generation Wireless (5G/6G) and P2P Blockchain

Prof. Latif Ladid

Université du Luxembourg

6:15 – 7:15 PM (CET) | August 23, 2021

Latif Ladid is a Senior Researcher at SnT. He works on multiple European Commission Next Generation Technologies IST Projects:

6INIT, www.6init.org - First Pioneer IPv6 Research Project; 6WINIT, Euro6IX, www.euro6ix.org ; Eurov6, www.eurov6.org ; NGNi, www.ngni.org ; Project initiator of SEINIT, www.seinit.org and SecurIST, www.securitytaskforce.org .

Latif initiated the new EU project u-2010 to research Emergency & Disaster and Crisis Management, www.u-2010.eu, re-launched the Public Safety Communication Forum, www.publicsafetycommunication.eu ,

supported the new IPv6++ EU Research Project called EFIPSANS, www.efipsans.org and the new safety & Security Project using IPv6 called Secricom, www.secricom.eu

and co-initiated the new EU Coordination of the European Future Internet Forum for Member States called ceFIMS: www.ceFIMS.eu.

He holds the following positions: President, IPv6 FORUM www.ip6forum.org, Chair, European IPv6 Task Force www.ipv6.eu , Emeritus Trustee, Internet Society www.isoc.org , Board Member IPv6 Ready & Enabled Logos Program and Board Member World Summit Award www.wsis-award.org .

Latif is also a Member of 3GPP PCG (www.3gpp.org), 3GPP2 PCG (www.3gpp2.org), Vice Chair, IEEE ComSoc EntNET (www.comsoc.org/~entnet/), Member of UN Strategy Council, member of IEC Executive Committee, Board member of AW2I, Board Member of Nii Quaynor Institute for Research in Africa, and member of the Future Internet Forum EU Member States, representing Luxembourg: http://ec.europa.eu/information_society/activities/foi/lead/fif/index_en.htm .

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Tutorial: Inference on the Edge with Tiny Deep Neural Networks

Andrea Calimera, PhD

Politecnico di Torino, Italy

Daniele Jahier Pagliari, PhD

Politecnico di Torino, Italy

Valentino Peluso, PhD

Politecnico di Torino, Italy

1:00 – 3:00 PM (CET) | August 24, 2021

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Abstract

This tutorial provides a comprehensive review of the training and optimization methods for tiny Deep Neural Networks (DNNs). Specifically, it aims to give a deep insight of what designers can do today to improve the efficiency of DNNs when the target is the offloading into embedded platforms powered by low-power, general-purpose cores commonly adopted at the edge of the Internet-of-Things. The first part gives an overview of the AIoT ecosystem, the available market and the strategic verticals. By introducing the contents of the tutorial and their taxonomy, we also discuss the technical challenges and the main figures-of-merit of practical use-cases belonging to some of our research projects. The second part covers the static optimization methods used at training time to squeeze DNNs and let them fit resource- constrained devices, like mobile CPUs and MCUs of the Cortex family by ARM. Traditional techniques, such as quantization and pruning, but also more recent strategies based on net-/operator-topology restructuring, will be introduced and assessed. The third and last part introduces dynamic optimization methods, a more recent branch of optimization strategies thought to give DNNs the ability to adapt to the surrounding context at run-time and implement speculative policies for resources minimization.

Andrea Calimera, PhD

Andrea Calimera is Associate Professor of Computer Engineering at Politecnico di Torino, Torino, Italy. Prior to that, he was Assistant Professor at the same institution. He received an MSc in Electronic Engineering and a PhD in Computer Engineering, both from Politecnico di Torino. His research interests cover the areas of Electronic Design Automation of digital circuits and embedded systems with emphasis on optimization techniques for low-power and reliable circuits and systems, dynamic energy/quality management, logic synthesis for emerging devices, design flows and methodologies for the efficient processing of machine learning and deep learning algorithms. He was visiting professor in Singapore, first at the School of Electrical and Computer Engineering of the National University of Singapore and then at the School of Computer Science and Engineering of the Nanyang Technological University of Singapore, contributing to research projects in the field of design automation for ultra-low power digital ICs and emerging technologies. Andrea Calimera is member of the International Federation for Information Processing (IFIP) and he has served on the technical program committee of many EDA and VLSI conferences, including the conference on Design and Test in Europe (DATE) and the International Conference on Computer Aided Design (ICCAD). He is member of the IEEE CAS society, Associate Editor of the IEEE Transactions on Circuits and Systems II, Associate Editor of the MDPI AI Journal.

Daniele Jahier Pagliari, PhD

Daniele Jahier Pagliari is an Assistant Professor at the Department of Control and Computer Engineering of Politecnico di Torino. He received the Ph.D. in Computer and Control Engineering from Politecnico di Torino. In 2012, Daniele was an intern at Istituto Nazionale di Ricerca Metrologica (INRIM) in Turin (IT), where he worked on the FPGA acceleration of digital synthesis algorithms for a high precision signal generator. In 2014, he was a visiting researcher at Columbia University in New York City (US), working on the design of hardware accelerators for medical imaging algorithms using High Level Synthesis. In 2016, he was a visiting researcher at the CEA Leti research center in Grenoble (FR), where he worked on the development of CAD and technological solutions for the design of scalable-precision digital arithmetic hardware for DSP and machine/deep learning applications. Daniele's research interests are in the field of Computer Aided-Design of digital circuits and systems. Recently, his main research focus has been on techniques and tools for the deployment and optimizations of deep learning algorithms on embedded devices. Daniele is a member of the IEEE.

Valentino Peluso, PhD

Valentino Peluso is a Post-doc Research Fellow in the Computer and Control Engineering Department at Politecnico di Torino. He received the M.S. degree in Electronic Engineering with honors from Politecnico di Torino in 2015. During his studies, he joined the “Alta Scuola Politecnica”, a two-year program restricted to 150 master students belonging to Politecnico di Torino and Politecnico di Milano. In February 2016, he joined the EDA group in Politecnico di Torino as a research assistant. In May, he started the Ph.D. program in Computer Engineering at the same research group and in September 2020 received the Ph.D. degree. His main research interests focus on AI-based applications for low-power systems, specifically, on the development of automation tools for the training, optimization and compression of neural networks that can be deployment on embedded microcontrollers and mobile CPUs. Valentino is a member of the IEEE.

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Keynote: Scaling Blockchains

Prof. A. Senhaji Hafid

University of Montreal

6:15 – 7:15 PM (CET) | August 25, 2021

Blockchain is a promising and revolutionary technology that has the potential to impact almost all industry segments. However, scalability is emerging as one the key challenging issues to its wide adoption. This talk will overview existing solutions to Blockchain scalability, which can be classified into two categories: First layer and second layer solutions. First layer solutions propose modifications to the Blockchain (i.e., changing the Blockchain structure, such as block size) while second layer solutions propose mechanisms that are implemented outside of the Blockchain. We will focus on sharding as a promising first layer solution to the scalability issue; in particular, we will investigate the trade-off between security and scalability of sharding-based blockchain protocols.

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Bio

Abdelhakim Senhaji Hafid is Full Professor at the University of Montreal. He is the founding director of Network Research Lab and Montreal Blockchain Lab. He is research fellow at CIRRELT, Montreal, Canada. He is also the co-chair of WG on Scalable Blockchains and Parachains; this WG is under IEEE TEMS TC on Blockchain and Distributed Ledger Technologies. Prior to joining U. of Montreal, he spent several years, as senior research scientist, at Bell Communications Research (Bellcore), NJ, US working in the context of major research projects on the management of next generation networks. Dr. Hafid consulted for a number of telecommunication companies and startups in North America; he also gave talks/keynotes in a number of international conferences. He co-founded Tipot Technologies Inc. (Research & Development Platform for IoT). Dr. Hafid has extensive academic and industrial research experience in the area of the management and design of next generation networks. His current research interests include IoT, Fog/edge computing, Blockchain, and intelligent transport systems.

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Hyperdimesional Computing: From Efficient Classifiers to General AI

Dr. Abbas Rahimi

IBM Research-Zürich laboratory, Switzerland

2:00 – 3:00 PM (CET) | August 25, 2021

Abbas Rahimi received the B.S. degree in computer engineering from the University of Tehran, Tehran, Iran, in 2010, and the M.S. and Ph.D. degrees in computer science and engineering from the University of California San Diego, La Jolla, CA, USA, in 2015, followed by postdoctoral researches at the University of California Berkeley, Berkeley, CA, USA, and at the ETH Zürich, Zürich, Switzerland. In 2020, he has joined the IBM Research-Zürich laboratory in Rüschlikon, Switzerland, as a Research Staff Member. Dr. Rahimi received the 2015 Outstanding Dissertation Award in the area of "New Directions in Embedded System Design and Embedded Software" from the European Design and Automation Association, and the ETH Zürich Postdoctoral Fellowship in 2017. He was a co-recipient of the Best Paper Nominations at DAC (2013) and DATE (2019), and the Best Paper Awards at BICT (2017) and BioCAS (2018).

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Tutorial: Privacy and Security Challenges for Machine Learning in IoT Devices

Francesco Regazzoni

University of Amsterdam, Netherlands

Paolo Palmieri

University College Cork, Ireland

7:30 – 8:30 PM (CET) | August 25, 2021

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Talk 1: Secure and Private Data Sharing in Complex Multi-Tenant Settings Speaker: Paolo Palmieri

Artificial Intelligence has achieved outstanding results in a number of fields, including speech and image recognition, autonomous cars, and health care. However, these progresses come at a cost. The large amount of data used to train the models used inside Artificial Intelligence algorithm can be, at least potentially, misused and ultimately create serious privacy risks. Concerns are also related to the protection of the trained models. The performance of an Artificial Intelligence model is, in fact, generally the outcome of complex and costly design and training processes. These trained model needs thus to be protected from piracy and from illegitimate use. These issues have not yet been fully addressed by the scientific community, as research on Artificial Intelligence is mostly focusing on improving performance and accuracy in achieving the desired task. However, with the increase of performance, especially of Deep Neural Networks, and in the changing landscape of AI deployment (where learning is increasingly carried out on the edge), comes a renewed need to address the challenges of privacy, and IP protection. Privacy issues can be addressed by executing learning and data analysis algorithms on encrypted data, and by employing a federated approach. Finally IP protection mechanisms, derived from the ones adopted for digital right management, can be applied to Artificial Intelligence models, and in particular to Deep Neural Networks to mitigate piracy problems. In a view of the increasing relevance of these issues, this tutorial will cover implications of novel privacy threats and security aspects related to Artificial Intelligence. The first talk will discuss the need of making AI applications robust, secure and privacy-preserving in complex multi-tenant settings (where different parties who do not necessarily trust each other want to collaborate), especially in the Internet of Things domain. The talk will summarize recent results on encryption for artificial intelligence, and analyze the benefits of federated learning from a privacy-preservation perspective.

Talk 2: Watermarking and protection of ML models

Artificial Intelligence has achieved outstanding results in a number of fields, including speech and image recognition, autonomous cars, and health care. However, these progresses come at a cost. The large amount of data used to train the models used inside Artificial Intelligence algorithm can be, at least potentially, misused and ultimately create serious privacy risks. Concerns are also related to the protection of the trained models. The performance of an Artificial Intelligence model is, in fact, generally the outcome of complex and costly design and training processes. These trained model needs thus to be protected from piracy and from illegitimate use. These issues have not yet been fully addressed by the scientific community, as research on Artificial Intelligence is mostly focusing on improving performance and accuracy in achieving the desired task. However, with the increase of performance, especially of Deep Neural Networks, and in the changing landscape of AI deployment (where learning is increasingly carried out on the edge), comes a renewed need to address the challenges of privacy, and IP protection. Privacy issues can be addressed by executing learning and data analysis algorithms on encrypted data, and by employing a federated approach. Finally IP protection mechanisms, derived from the ones adopted for digital right management, can be applied to Artificial Intelligence models, and in particular to Deep Neural Networks to mitigate piracy problems. In a view of the increasing relevance of these issues, this tutorial will cover implications of novel privacy threats and security aspects related to Artificial Intelligence. The second talk will present watermarking and fingerprinting techniques used to protect Deep Neural Networks from illegitimate use of trained models (for instance when an adversary uses a model without obtaining the needed licenses). The talk will report recent achievement on watermarking and fingerprinting in such do- main an presents the most relevant attacks against these protection mechanisms.

Francesco Regazzoni

Francesco Regazzoni is assistant professor at University of Amsterdam (Amsterdam, The Nether- lands) and group leader at the Università della Svizzera italiana (Lugano, Switzerland). He received his Master of Science degree from Politecnico di Milano and his PhD degree at the ALaRI Institute of University of Lugano. He has been assistant researcher at the Université Catholique de Louvain and at Technical University of Delft, and visiting researcher at several institutions, including NEC Labs America, Ruhr University of Bochum, EPFL, and NTU Singapore. His research interests are mainly focused on embedded systems security, covering in particular side channel attacks, electronic design automation for security, hardware Trojans, and low energy cryptography. He has published more than 100 peer reviewed journal and conference papers in the area of security and design automation, (including CHES, NDSS, EUROCRYPT, ASIACRYPT, DAC, DATE, HOST and ASP- DAC), has been in the technical program committed of top conferences of the area (including CHES, DATE, DAC, ICCAD, HOST), and he chaired the program committee of COSADE and FDTC.

Paolo Palmieri

Dr. Paolo Palmieri is a Lecturer (above the bar) in Cyber Security at the School of Computer Science & IT at UCC. He earned his PhD at the Crypto Group of the Université catholique de Louvain (Belgium) in 2013, and before joining UCC in September 2017 he had been a Lecturer in Cyber Security at Cranfield University (UK), a Lecturer in Computing at Bournemouth University (UK), and Post-Doctoral Researcher at Delft University of Technology (Netherlands). He is a Funded Investigator in CONNECT – the Irish Research Centre for Future Net- works, and Insight – the Irish Research Centre for Data Analytics, and he is also an External Affiliate of the Smart City Lab at the University of Bologna (Italy). His research focuses on cryptographic protocol for security and privacy, and he was the first to propose a protocol achieving secure multi-party computation on communication delays. His work on location privacy and secure cooperative computation of location information has been implemented a number of times and is currently used in real-world applications, including satellite monitoring and smart transportation. He has significant track record in hash-based probabilistic data structures and approximated cryptographic primitives.

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Keynote: Wireless Transmissions for Green Internet of Things: Session-specific Analysis and Design

Prof. Hong-Chuan Yang

University of Victoria

7:30 – 8:30 PM (CET) | August 24, 2021

Wireless communication systems will play an essential role in data transmission for future Internet of Things (IoT). Since most IoT devices have limited energy supply, developing highly energy-efficient wireless transmission strategies for various IoT application scenarios are of critical practical, economical, and environmental interests. Following the recently proposed data-oriented approach, in this talk, we analyze and optimize wireless transmission systems from individual session perspective. We characterize the energy efficiency performance limits for individual IoT transmission sessions, subject to reliability and latency constraints. We also study the optimal design in terms of energy consumption minimization for various scenarios, including relay transmission with wireless energy transfer and remote data collection through unmanned aerial vehicles (UAV). Finally, we demonstrate the potential applications of advanced machine learning algorithms in the session-specific wireless transmission system design.

http://coinsconf.com

Bio

Prof. Hong-Chuan Yang received the Ph.D. degree in Electrical Engineering from the University of Minnesota, Minneapolis, USA, in 2003. Dr. Yang is a professor of the Department of Electrical and Computer Engineering at the University of Victoria, Victoria, Canada. From 1995 to 1998, he was a Research Associate with the Science and Technology Information Center (STIC) of Ministry of Posts & Telecommunications (MPT), Beijing, China. His research focuses on different aspects of wireless communications, with special emphasis on the analysis and design of advanced transmission technologies for future Internet of Things (IoT). Dr. Yang has published over 200 referred journal and conference papers. He is the author of the book Introduction to Digital Wireless Communications (IET Publishing) and the co-author of the books Advanced Wireless Transmission Technologies and Order Statistics in Wireless Communications (Cambridge Univ. Press). Dr. Yang is a senior member of IEEE and a registered professional engineer in BC, Canada.

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Tutorial: Approximate and Reliable Computing for Machine Learning and Safety-Critical Systems

Dr. Jie Han

University of Alberta, Canada

Dr. Weiqiang Liu

Nanjing University of Aeronautics and Astronautics, China

Dr. Alberto Bosio

University of Lyon - Lyon Institute of Nanotechnology, France

3:15 – 4:15 PM (CET) | August 25, 2021

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Talk 1: Approximate Computing for Safety-Critical Applications

Today, the concept of approximation in computing is becoming more and more a “hot topic” to investigate how computing systems can be more energy-efficient, faster, and less complex. Intuitively, instead of performing exact computations and, consequently, requiring a high amount of resources, Approximate Computing aims at selectively relaxing the specifications, trading accuracy off for efficiency. While Approximate Computing allows many improvements when looking at systems' performance, energy efficiency and complexity, it poses significant challenges regarding the test and the in-field reliability of Approximate Digital Integrated Circuits especially when the final target is a Safety-Critical application. The talk will also present how approximate computing can be successfully applied to design low cost fault tolerant/detection mechanisms for Safety-Critical applications.

Talk 2: Approximate Computing: Machine Learning Applications and Security

Approximate computing has been proposed for highly energy efficient systems targeting the emerging error tolerant applications. Approximate computing consists of approximately (inexactly) processing data to save power and achieve high performance, while results remain at an acceptable level for subsequent use. In this talk, I will focus on the applications of approximate computing into machine learning applications including adaptive approximate computing for supervised and unsupervised scenarios, deep neural network accelerator using approximate multipliers and the approximate designs of key components such as softmax. Furthermore, the application of approximate computing into security and cryptography as well as the security issue in approximate computing itself are also considered.

Talk 3: A Review and Characterization of Approximate Arithmetic Circuits for Approximate Computing

Approximate computing is emerging as a new paradigm for high-performance and energy-efficient design of circuits and systems. This part of the tutorial aims to provide a review and characterization of recently proposed approximate arithmetic circuits under different design constraints. Specifically, approximate adders, multipliers and dividers are characterized via synthesis under optimizations for performance and area, respectively. The error and circuit characteristics are then generalized for different classes of designs. The applications of these circuits in image processing and deep neural networks indicate that such computations are more sensitive to errors in addition than those in multiplication, so a larger approximation can be tolerated in multipliers than in adders. The use of approximate arithmetic circuits can improve the quality of image processing and deep learning in addition to the benefits in performance and power consumption for these applications.

Jie Han

Jie Han received the B.Sc. degree in electronic engineering from Tsinghua University, Beijing, China, in 1999 and the Ph.D. degree from the Delft University of Technology, The Netherlands, in 2004. He is currently a Professor in the Department of Electrical and Computer Engineering at the University of Alberta, Edmonton, AB, Canada. His research interests include approximate computing, stochastic computing, reliability and fault tolerance, nanoelectronic circuits and systems, novel computational models for nanoscale and biological applications.

Dr. Han was a recipient of the Best Paper Award at the International Symposium on Nanoscale Architectures (NanoArch) 2015 and Best Paper Nominations at the 25th Great Lakes Symposium on VLSI (GLSVLSI) 2015, NanoArch 2016 and the 19th International Symposium on Quality Electronic Design (ISQED) 2018. He was nominated for the 2006 Christiaan Huygens Prize of Science by the Royal Dutch Academy of Science. His work was recognized by Science, for developing a theory of fault-tolerant nanocircuits (2005).

He is currently an Associate Editor for the IEEE Transactions on Emerging Topics in Computing (TETC), the IEEE Transactions on Nanotechnology, the IEEE Circuits and Systems Magazine, the IEEE Open Journal of the Computer Society, and Microelectronics Reliability (Elsevier Journal). He served as a General Chair for GLSVLSI 2017 and the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2013, and a Technical Program Committee Chair for GLSVLSI 2016, DFT 2012 and the Symposium on Stochastic & Approximate Computing for Signal Processing and Machine Learning, 2017.

Weiqiang Liu

Weiqiang Liu is currently a Professor and the Vice Dean of College of Electronic and Information Engineering, Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China.
He received the B.Sc. degree in Information Engineering from NUAA and the Ph.D. degree in Electronic Engineering from Queen's University Belfast (QUB), Belfast, United Kingdom, in 2006 and 2012, respectively.
His research interests include approximate computing, computer arithmetic, hardware security, VLSI design for DSP and cryptography, and mixed-signal integrated circuit.
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He has served as a Steering Committee Member of IEEE TVLSI, Associate Editors of IEEE TCAS-I, TETC, TC, a Guest Editor of Proceedings of the IEEE. He is the Program Co-Chair of IEEE ARITH, and program members for a number of international conferences. He is a speaker of the ISCAS 2021 half-day tutorial. He is a Senior Member of the IEEE, CIE and CCF.

Alberto Bosio

Alberto Bosio received the Ph.D. in Computer Engineering from the Politecnico di Torino, Italy in 2006. From 2007 to 2018 he was an Associate Professor at LIRMM - University of Montpellier in France. From September 2018 he joined the INL - Ecole Centrale de Lyon, France as Full Professor. His research interests include Approximate Computing, In-Memory Computing, Test and Diagnosis of Digital circuits and Reliability Assessment.

He is co-author of 1 book and 1 book-chapter, 4 patents, 42 papers in international journals and more than 130 papers in international conferences and workshops.

He serves as member of the program committee of several international conferences and reviewers for several journals. He is also European Test Technology Technical Council (ETTTC) chair.

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Tutorial: Algorithm-Circuits-Device Co-design for Edge Neuromorphic Intelligence

Dr. Abbas Rahimi

IBM Research-Zürich laboratory, Switzerland

6:15 – 7:15 PM (CET) | August 24, 2021

Melika Payvand is a research scientist at the Institute of Neuroinformatics, University of Zurich and ETH Zurich. She received her M.S. and Ph.D. degree in electrical and computer engineering from the University of California Santa Barbara in 2012 and 2016 respectively. Her research activities and interest is in exploiting the physics of the computational substrate for online learning and sensory processing on the edge. She is co-coordinating the European NEUROTECH project and is in the scientific committee of the Capocaccia workshop for neuromorphic intelligence. She is serving as the chair for the neural network and neuromorphic engineering track at the IEEE flagship conference International Conference in Circuits and Systems (ISCAS), and is in the technical committee of Neural Systems, Applications and Technologies in Circuits and System society. She is a guest editor of Frontiers in Neuroscience and is the winner of the best neuromorph award of the 2019 Telluride neuromorphic workshop. Her research has resulted in more than 30 peer reviewed journal articles, book chapters and conference proceedings.

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Tutorial: Challenges and Solutions for Flight Duration Enhancement in UAV Wireless Networks

Prof. Mohamed-Slim Alouini

King Abdullah University of Science and Technology (KAUST)

Dr. Mustafa A. Kishk

King Abdullah University of Science and Technology (KAUST)

2:00 – 4:15 PM (CET) | August 26, 2021

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Abstract

Drone-mounted base-stations (DBSs) have a great potential to enhance wireless coverage and data rate of IoT networks, as well as other applications such as data dissemination and collection. However, one of the main challenges in such technology is the limited on-board battery. The limited energy resources lead to a drone flight time that typically does not exceed one hour. Hence, the drone needs to frequently fly back to a charging station to replace/recharge its battery. During this time, the quality of service (QoS) experienced by the users in the coverage area of the drone might degrade. Hence, it is necessary to find innovative solutions that enable a longer drone flight time, in order to ensure a stable wireless coverage provided by the users. In this tutorial, we first discuss the general advantages and potential use cases of DBSs. Next, we discuss the limited drone battery influence on the performance of the drone- enabled wireless network. In particular, we discuss a stochastic geometry-based framework that accurately captures the influence of the battery size, the density of the charging stations, and the required charging time on the performance of the wireless network. Next, we enlist a set of potential solutions that have the potential to extend the flight time of DBSs with emphasis on: (1) tethered drones and (2) laser-powered drones. For each of the two solutions, we first briefly discuss the technology state of the art. Next, we provide a set of open research directions for these novel system architectures that require revisiting many well-established results in the literature of drone-enabled wireless networks analysis.

Mohamed-Slim Alouini

Mohamed-Slim Alouini [S'94-M'98-SM'03-F'09] was born in Tunis, Tunisia. He received the Ph.D. degree in Electrical Engineering from the California Institute of Technology (Cal- tech), Pasadena, CA, USA, in 1998. He served as a faculty member in the University of Minnesota, Minneapolis, MN, USA, then in the Texas A&M University at Qatar, Education City, Doha, Qatar before joining King Abdullah University of Science and Technology (KAUST), Thuwal, Makkah Province, Saudi Arabia as a Professor of Electrical Engineering in 2009. His current research interests include the modeling, design, and performance analysis of wireless communication systems.

Mustafa A. Kishk

Mustafa A. Kishk [S'16, M'18] is a postdoctoral research fellow in the communication theory lab at King Abdullah University of Science and Technology (KAUST). He received his B.Sc. and M.Sc. degree from Cairo University in 2013 and 2015, respectively, and his Ph.D. degree from Virginia Tech in 2018. His current research interests include stochastic geometry, energy harvesting wireless networks, UAV-enabled communication systems, and satellite communications.